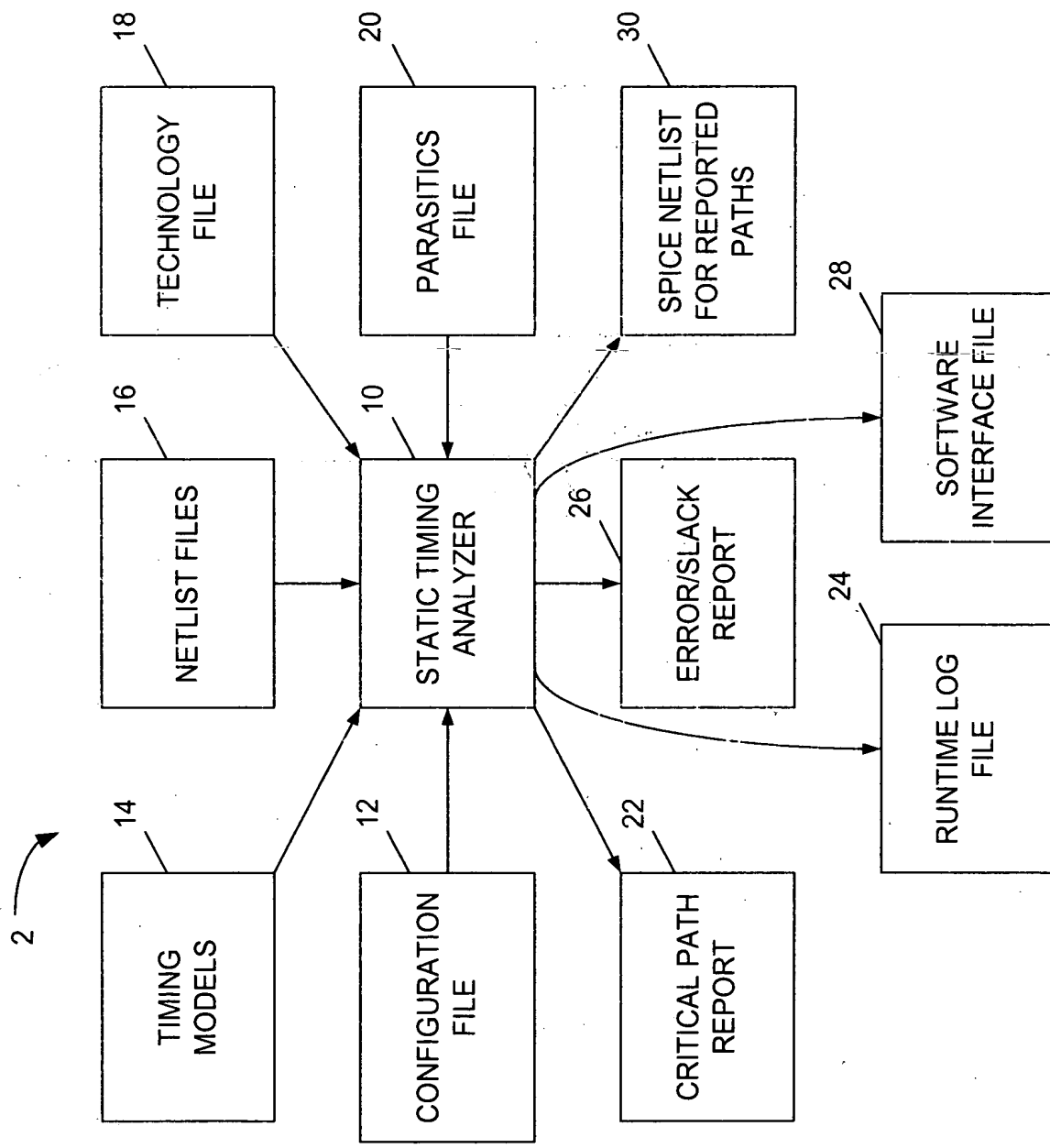


**FIG. 1**  
(PRIOR ART)



**FIG. 2**

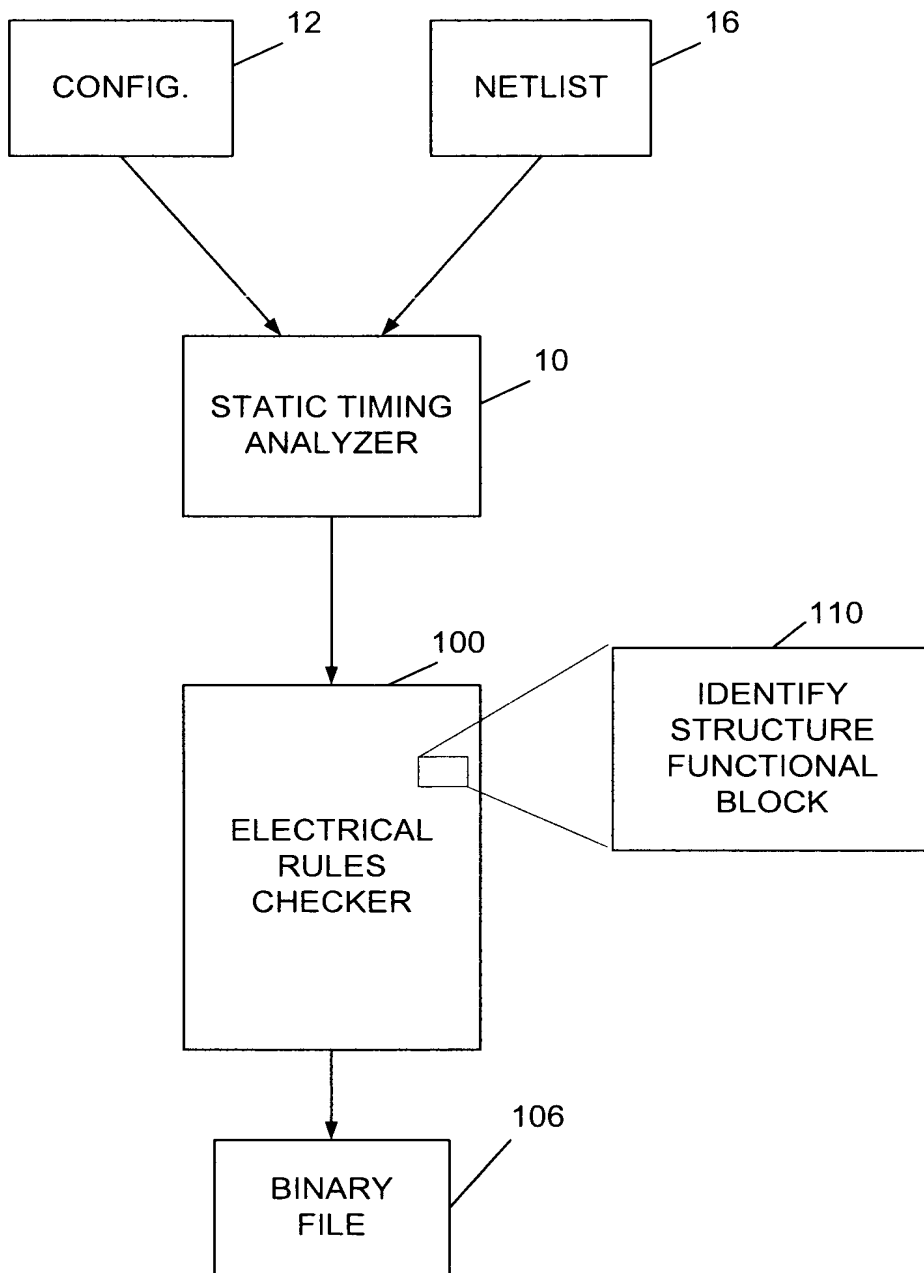
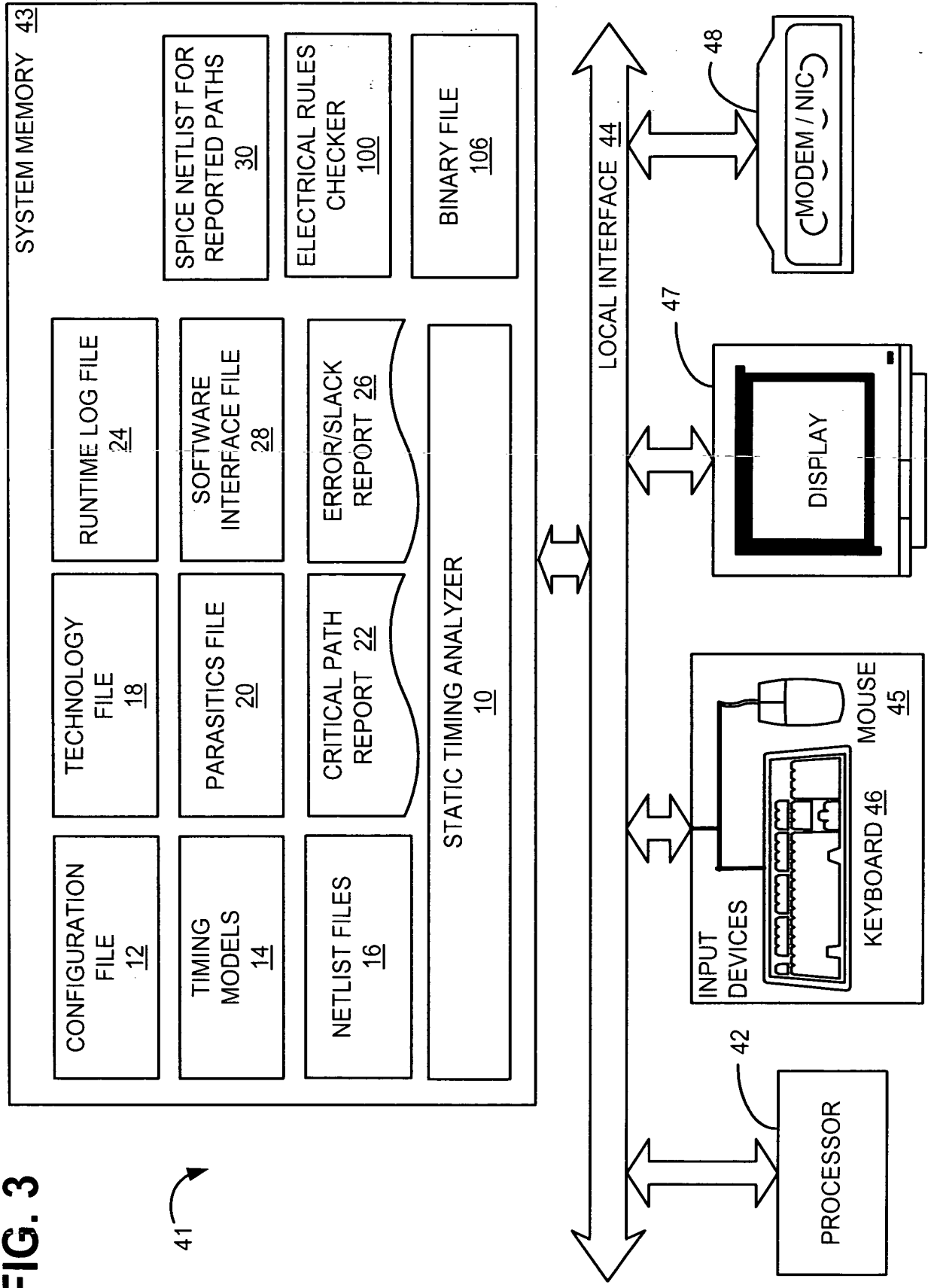


FIG. 3



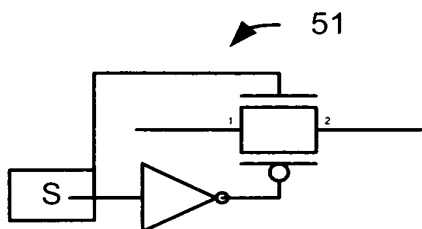
## FIG. 4A

ELEMENT {~~~~  
~~~~  
Complementary Pass FET  
Special Complementary Pass FET  
RAM Cells  
Single Pass FET  
Feedback FET  
Static Gates  
Probable  
~~~~~  
~~~~~  
Direction: Unset, Bidirectional, Source-to-  
Drain, Drain-to-Source,  
~~~~~}

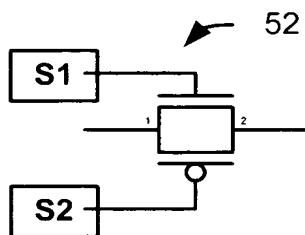
## FIG. 4B

NODE {~~~~  
~~~~  
Output  
Inverter Outputs  
Latch  
Precharged  
Dynamic  
Static  
Clock driver  
Mux Output  
~~~~~  
~~~~~}

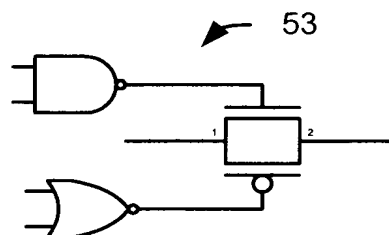
**FIG. 5A**



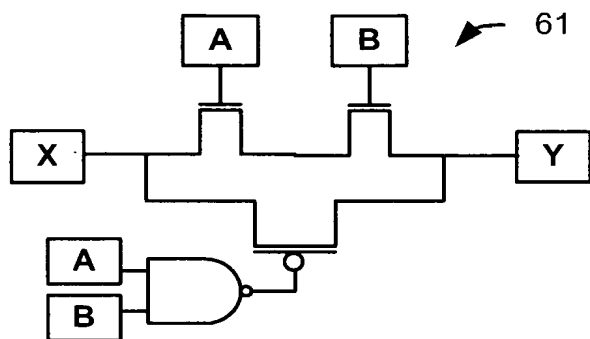
**FIG. 5B**



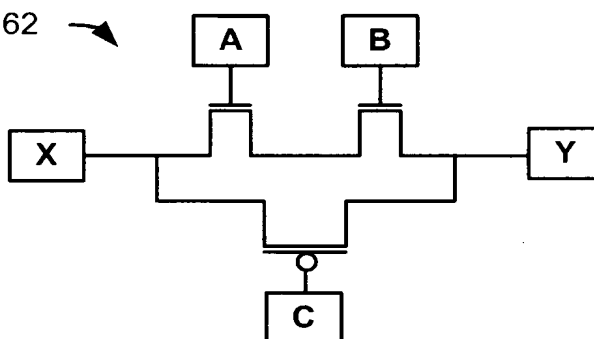
**FIG. 5C**



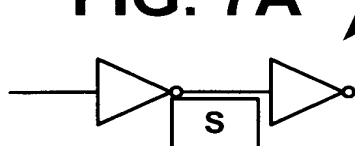
**FIG. 6A**



**FIG. 6B**



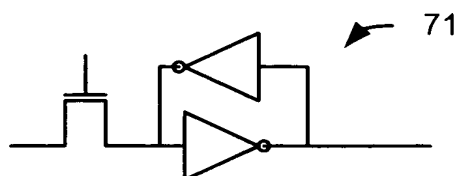
**FIG. 7A**



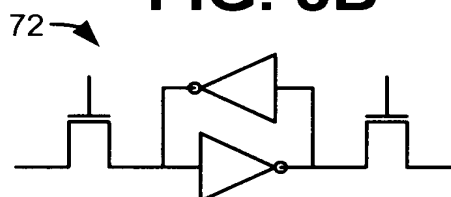
**FIG. 7B**



**FIG. 8A**



**FIG. 8B**



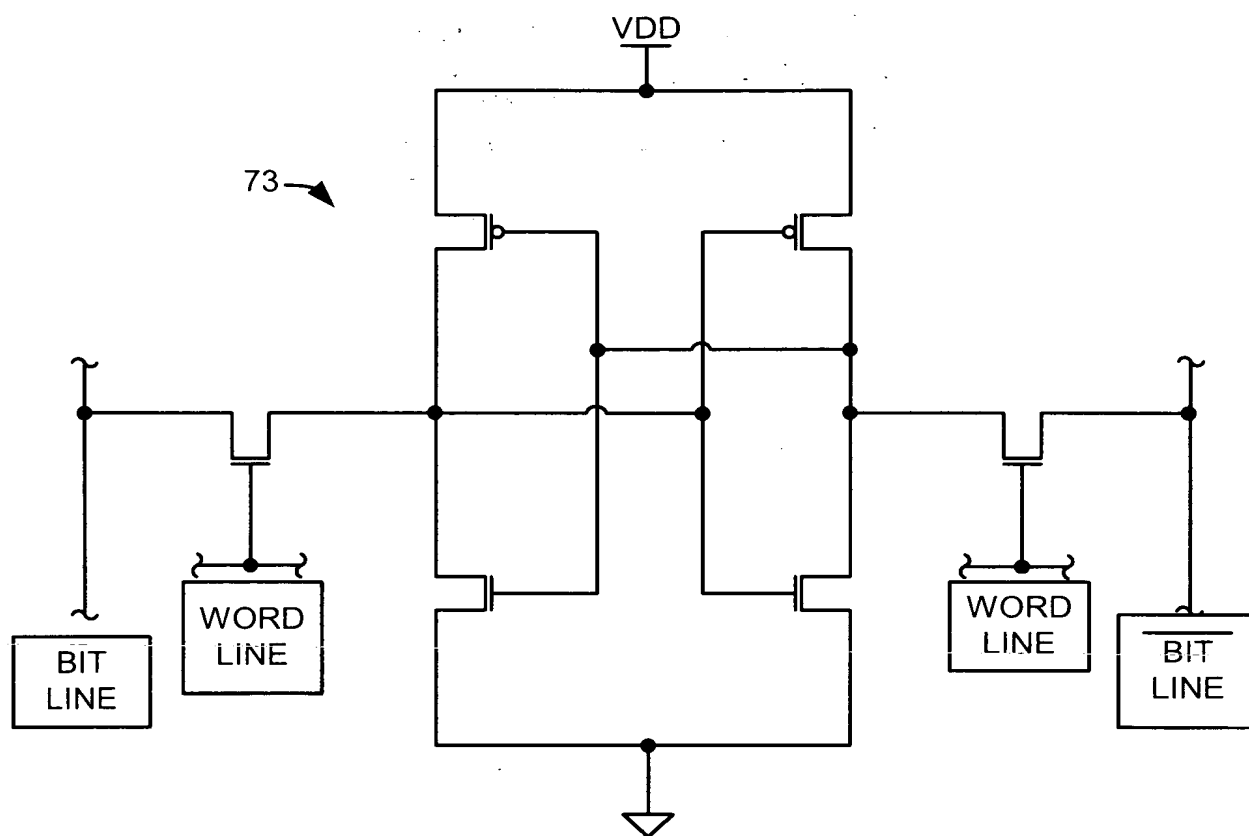


FIG. 9

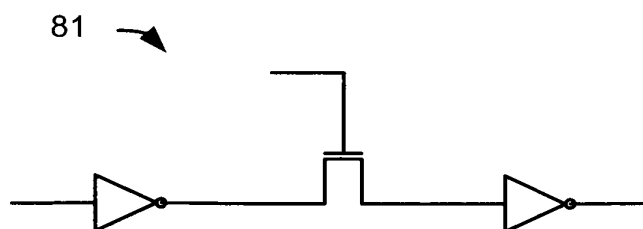


FIG. 10A

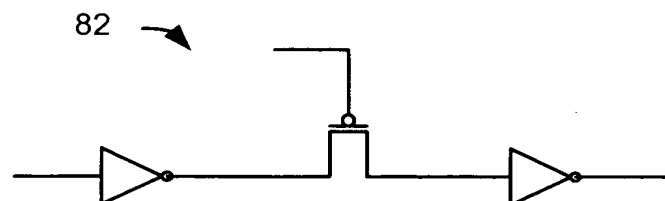


FIG. 10B

**FIG. 11**

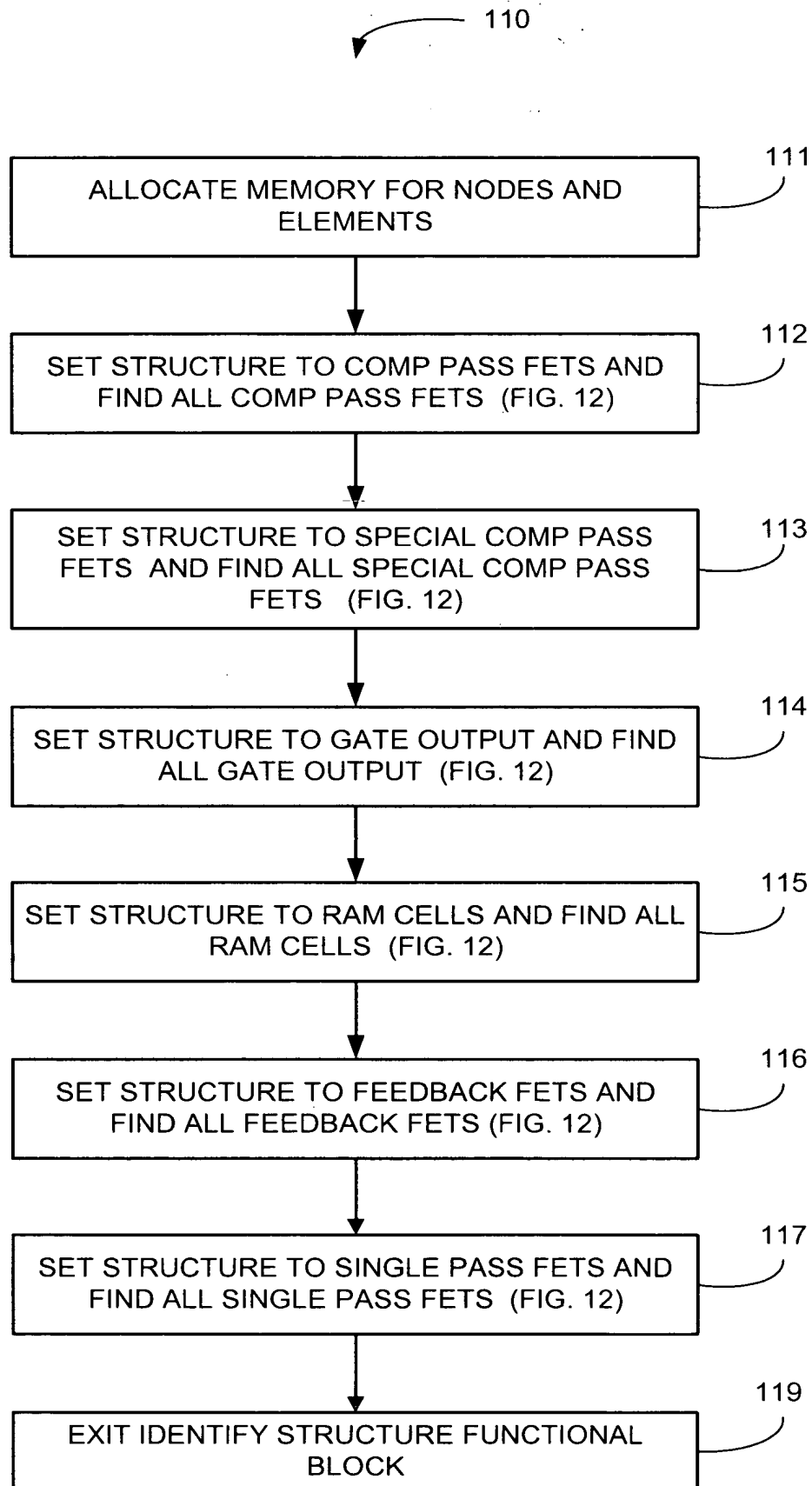
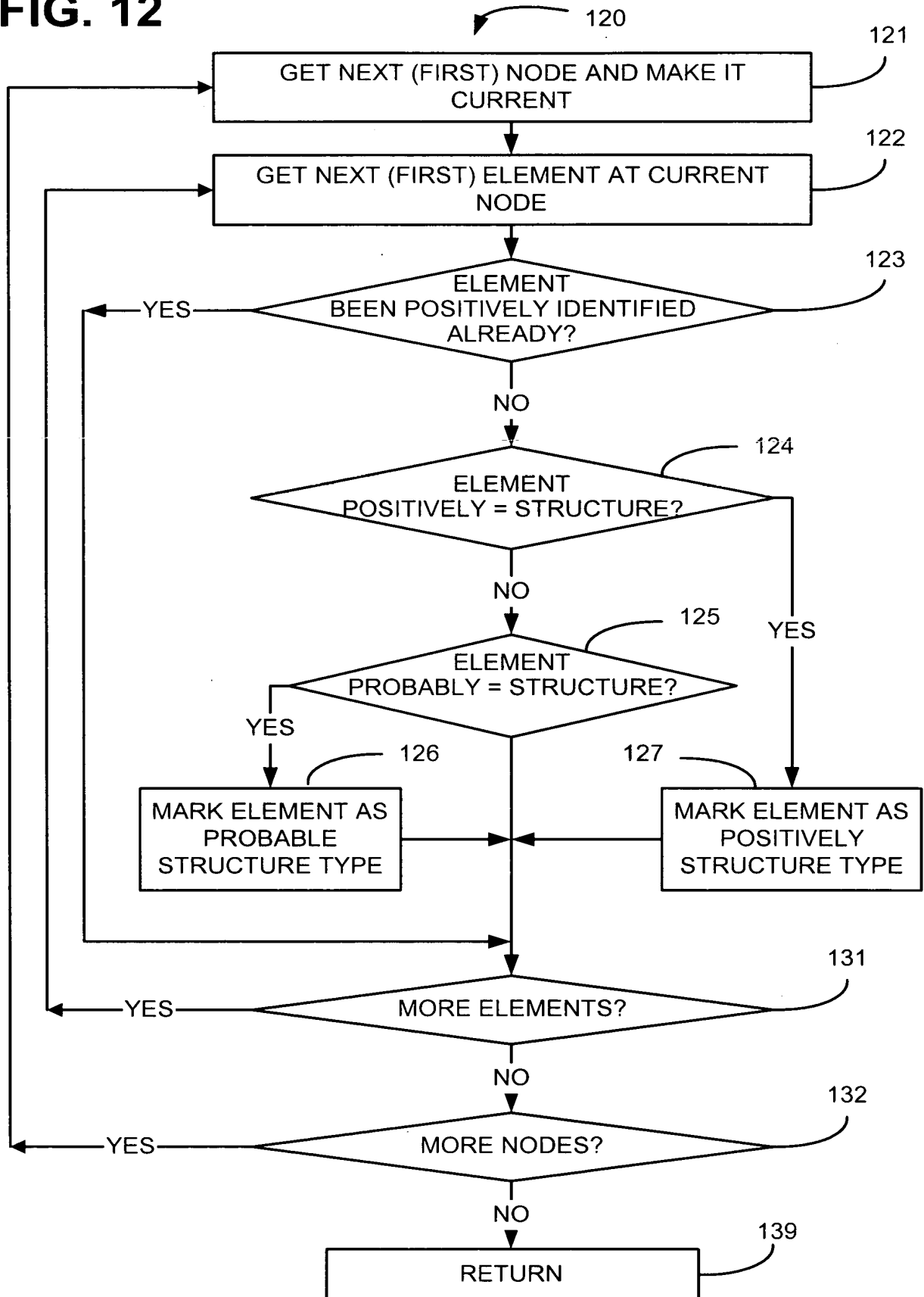


FIG. 12



005700" 07960000